CLAIMS

What is claimed is:

1. An electrical device comprising:

a semiconductor substrate having a top surface;

a gate region over the semiconductor substrate, wherein the gate region has a bottom surface that is substantially parallel to the top surface of the semiconductor substrate;

an electrical insulation layer over the top surface of the semiconductor substrate and upon the gate region; and

at least one source/drain region for the gate region and situated within the semiconductor substrate, wherein:

the source/drain region has a first portion that extends from the top surface of the semiconductor substrate to a bottom periphery and has a concentration of dopant of greater than about 1x1019 dopant atoms per cm3;

the source/drain region has a second portion that extends from the bottom periphery of the first portion and has a concentration of dopant of less than about 1x1019 dopant atoms per cm3;

the first portion of the source/drain region does not underlap the bottom surface of the gate region that is substantially parallel to the top surface of the semiconductor substrate; and

the second portion of the source/drain region underlaps the bottom surface of the gate region that is substantially parallel to the top surface of the semiconductor substrate.

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2. The electrical device of claim 1, wherein the semiconductor substrate is composed of silicon.

3. The electrical device of claim 1, wherein the electrical insulation layer comprises tetraethyl orthosilicate.

4. The electrical device of claim 1, wherein the second portion of the source/drain region has a lower periphery that is substantially parallel to the top surface of the semiconductor substrate.

5. The electrical device of claim 1, wherein the dopant comprises a material selected from the group consisting of boron and phosphorus.

6. The electrical device of claim 1, wherein the dopant is implanted in the first portion by a plasma doping operation and at least one other ion bombardment implantation operation without a plasma.

7. The electrical device of claim 6, wherein the dopant is implanted in the second portion by the ion bombardment implantation operation without a plasma.

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8. An electrical device comprising:

a semiconductor substrate having a top surface;

a gate insulation layer on the top surface of the semiconductor substrate;

a gate region on the gate insulation layer, wherein the gate region has a bottom surface that is substantially parallel to the top surface of the semiconductor substrate;

a first source/drain region for the gate region and within the semiconductor substrate;

a second source/drain region for the gate region and within the semiconductor substrate; and

an electrical insulation layer conformingly situated upon:

the gate region; and

the gate insulation layer;

wherein each of the first source/drain region and the second source/drain region include an inner portion and an outer portion, wherein:

the inner portion:

extends from the top surface of the semiconductor substrate to a bottom periphery;

has a concentration of dopant of about 1x1019 to about 5x1021 dopant atoms per cm3; and

does not underlap the bottom surface of the gate region that is substantially parallel to the top surface of the semiconductor substrate; and

the outer portion:

is contiguous with the inner portion;

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extends from the bottom periphery of the inner portion;

underlaps the bottom surface of the gate region that is substantially parallel to the top surface of the semiconductor substrate; and

has a concentration of dopant of less than about 1x1019 dopant atoms per cm3.

9. The electrical device of claim 8, wherein the semiconductor substrate is composed of silicon.

10. The electrical device of claim 8, wherein the electrical insulation layer comprises tetraethyl orthosilicate.

11. The electrical device of claim 8, wherein each outer portion extends to terminate at a lower periphery that is substantially parallel to the top surface of the semiconductor substrate.

12. The electrical device of claim 8, wherein the dopant comprises a material selected from the group consisting of boron and phosphorus.

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13. An electrical device comprising:

a semiconductor substrate having a top surface;

a gate insulation layer on the top surface of the semiconductor substrate;

a spacerless gate region on the gate insulation layer, wherein the spacerless gate region has a bottom surface that is substantially parallel to the top surface of the semiconductor substrate;

a first source/drain region for the gate region and within the semiconductor substrate;

a second source/drain region for the gate region and within the semiconductor substrate; and

an electrical insulation layer conformingly situated over the top surface of the semiconductor substrate and upon the spacerless gate region;

wherein each of the first source/drain region and the second source/drain region include an inner portion and an outer portion, wherein:

the inner portion:

does not underlap the bottom surface of the gate region that is substantially parallel to the top surface of the semiconductor substrate;

extends from the top surface of the semiconductor substrate to a bottom periphery; and

has a concentration of dopant of about 1x1019 to about 5x1021 dopant atoms per cm3;

the outer portion:

underlaps the bottom surface of the gate region;

is contiguous with the inner portion;

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extends from the bottom periphery of the inner portion; and

has a concentration of dopant of less than about 1x1019 dopant atoms per cm3.

14. The electrical device of claim 13, wherein the semiconductor substrate is composed of silicon.

15. The electrical device of claim 13, wherein the electrical insulation layer comprises tetraethyl orthosilicate.

16. The electrical device of claim 13, wherein each outer portion extends within the semiconductor substrate to a lower periphery that is substantially parallel to the top surface of the semiconductor substrate.

17. The electrical device of claim 13, wherein the dopant comprises a material selected from the group consisting of boron and phosphorus.

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